ABSTRACT

A Viterbi decoder capable of supporting a variety of constraint lengths and any arbitrary number of coefficients of a given estimated transmission path and composed of special hardware of small circuit scale. In the Viterbi decoder of the present invention, a branch metric calculation section (101) calculates the branch metrics of all paths from the state of the previous time to the state at the present time, selects the most probable path from the paths arriving at respective states based on the branch metrics (101a) and path metrics (103a) and outputs path select signal (102a) and path metric (102b). Path metric storage section (103) outputs path metric (103a) to be input to ACS calculation section (102) when performing ACS calculating at the next time. Path select signal temporary storage section (104) holds path select signal (102a) of n states, outputs path select signal (104a) of m states ($m \leqq n$) and changes a bit input position according to the encoding constraint length or the number of coefficient of deduced estimated transmission path of the system which performs Viterbi decoding.